POWER HARDWARE IN THE LOOP SIMULATION

RTDS Technologies

Contents

1 Introduction to Hardware in the Loop (HIL) Simulations

In Hardware in the Loop (HIL) simulations, hardware devices are interfaced to a Real Time Simulator (RTS) which models the rest of the system used to test the device operation.

HIL simulations offer a cost-effective and safe method to test physical devices under real time operating conditions. Various contingency scenarios can be done in a controlled environment to evaluate the performance of the device under test (DUT) before it is connected to the actual physical system.

HIL simulations can be **open-loop** where signals are sent from the RTS to the device or most commonly **closed loop** where the response of the device is fed back to the RTS. HIL simulations are divided into two types: **Control** HIL (CHIL) and **Power** HIL (PHIL).

In CHIL, physical control or protection relay devices are interfaced with the RTS and exchange digital and/or analog signals as shown in Figure 1-1. In most CHIL applications, the signals can be exchanged at low voltage levels (±10V) allowing a straight forward interface with the RTDS using digital-analog (D/A) and analog-digital (A/D) converters. Some CHIL applications may require amplifiers to provide higher voltages and/or currents than provided by the D/A converter in the RTDS. In such applications, the loading of the amplifiers does not affect the stability and accuracy of the interface as the amplifier acts only as a power source i.e. 2 quadrant operation.

Recent advancements in some CHIL simulations use protocol based communication interfaces reducing the need for complex physical wiring and extensive hardware maintenance. CHIL applications have well established test standards and procedures and numerous examples have been well-documented in numerous technical literature and will not be discussed further in this document.

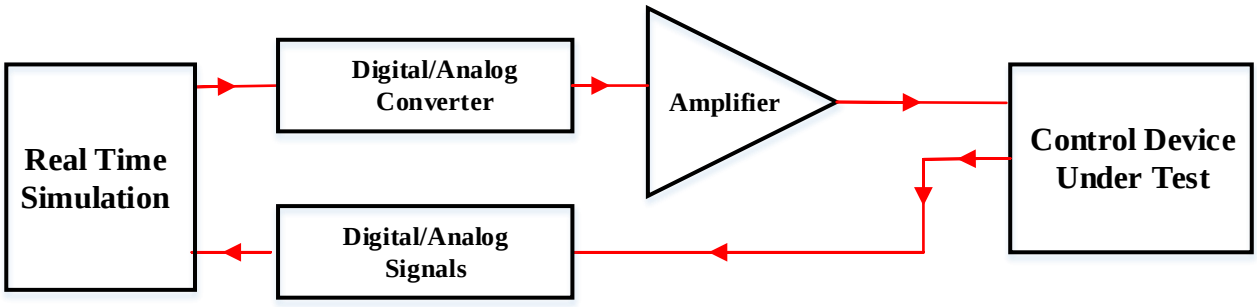

Figure 1-1 Control hardware in the loop simulations

2 Power Hardware in the Loop Simulations

PHIL simulations involves interfacing the RTS with a power device such as motors, inverters, generators and transformers. The RTS and the power device exchange power over the PHIL interface. The digital to analog (D/A) converters included as part of the RTDS provide analog signals scaled down to electronic levels within ±10Vpk. These voltage levels are well below the operating voltage/current range of the power device under test, therefore amplifiers are required in PHIL simulations to scale the signals sent from the RTDS to the DUT. PHIL simulations require more complex circuitry and hardware maintenance compared to CHIL applications. In addition, the interface between the RTDS and the device under test (DUT) is non-ideal due to time delays, noise and the limited bandwidth of the interface devices. These non-idealities impact the stability and accuracy of PHIL simulations and must be carefully considered for any PHIL simulation. The following sections discusses the key factors to be considered for PHIL simulations.

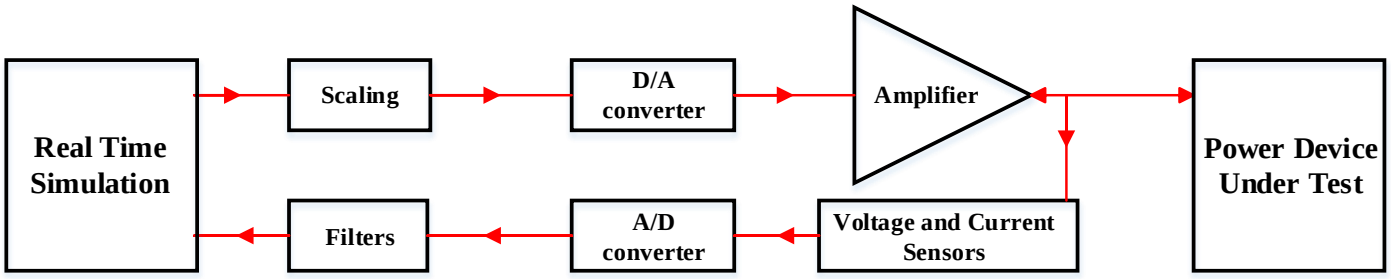

Figure 2-1 Power hardware in the loop simulations

2.1 Simulation Time Step

The time delay in the PHIL interface depends on the interface devices and is largely determined by the simulation time step in the RTDS. Ideally, the time step should be as small as possible to reduce delays in the HIL loop; however the required minimum time step is determined by the size of the simulated network in the RTDS. The small time step feature can be used to reduce the time delays in the PHIL simulation as the time step is kept between 1.4µsecs - 3µsecs; however stricter node limitations and limited model availability restrict the size of the simulated network that can be achieved in the small time step.

2.2 Amplifier

For closed loop PHIL simulations, the amplifier must be able to operate in all four quadrants of the power plane (i.e. they must be able to sink and source real and reactive power).

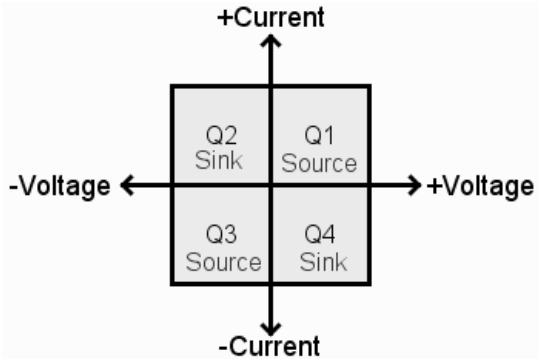

Figure 2-2 Four quadrant amplifier operation for PHIL simulations

Commonly used amplifiers are controlled voltage or controlled current amplifiers. Amplifiers capable of operating as both controlled voltage and controlled current can provide extended capability at a reduced cost.

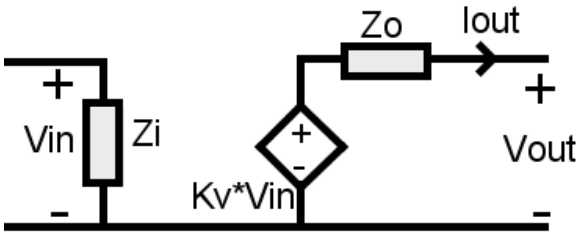

Figure 2-3 Controlled Voltage Amplifier

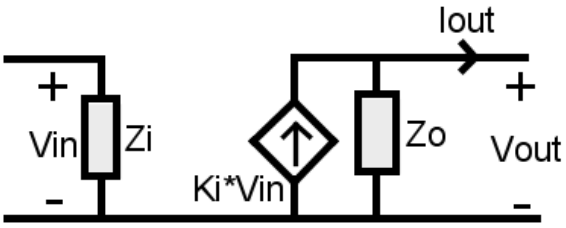

Figure 2-4 Controlled Current Amplifier

Where:

- Zi Input impedance of the amplifier
- Zo Output impedance of the amplifier
- Kv, Ki is the amplifier gain (voltage/current)

Depending on the application, amplifiers can be used for AC or DC operation. For DC operation, the input signal is directly coupled to the amplifier input. For AC operation, filters are used to eliminate the DC components in the input signal. AC operation is used to avoid DC saturation when testing transformers or motor devices. Amplifiers with DC or AC operation option provide extended capability for various PHIL applications. Table 2-1 lists a comparison of amplifiers used for PHIL simulations.

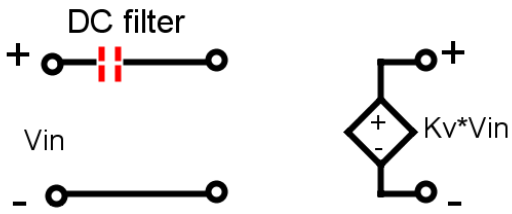

Figure 2-5 Filtering DC component from amplifier input

Table 2-1 Amplifiers for PHIL Simulation [Amplifier paper]

Amplifier operation	Definition	Complexity	Types and Manufacturer	Dynamic Response	Cost	Flexibility and Application Range
Linear	Change in output proportional to change in input	Low	Voltage or Current **Manufacturer:** Spitzenberger and Spies	High bandwidth and fast response time (<6µs)	High	Low flexibility (can operate only as voltage or current amplifier). Difficult to build in MW range due to high power losses.
Non-Linear	Change in output NOT proportional to change in input	High (Additional control circuitry required)	Switched mode **Manufacturer:** Triphase	Reduced bandwidth and slow response time (>50µs) (due to additional control circuitry)	Low	High Flexibility (can operate as voltage and/or current). Commonly used in the MW range.

The following characteristics must also be carefully considered to select the amplifier for the PHIL application:

- Power ratings of the device under test.
- Amplifier interface connections
- Source and sink power ratings of the amplifier.
- Amplifier response times.
- Amplifier slew rate.
- Amplifier harmonic distortion and frequency resolution.
- Amplifier input and output voltage/current range
- Amplifier input and output impedances

- Amplifier protection (overload, heating, short circuit operation)

The bandwidth of the amplifier represents the frequency range of the input signal the amplifier is effective at amplifying. The selected amplifier should have sufficient bandwidth to amplify the input signal at the frequencies of interest with minimum harmonic distortion. The bandwidth is usually specified from DC to the large signal response (-3dB bandwidth).

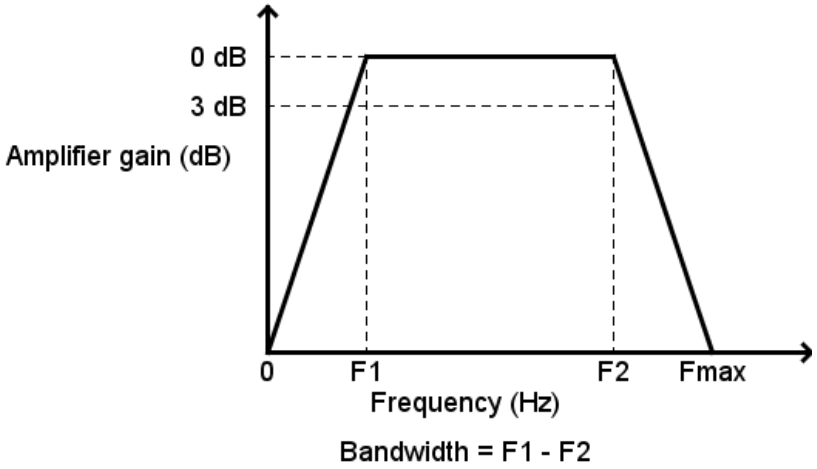

Figure 2-6 Amplifier Bandwidth

The amplifier response times and frequency behaviour can be characterized from its step response as shown in Figure 2-6.

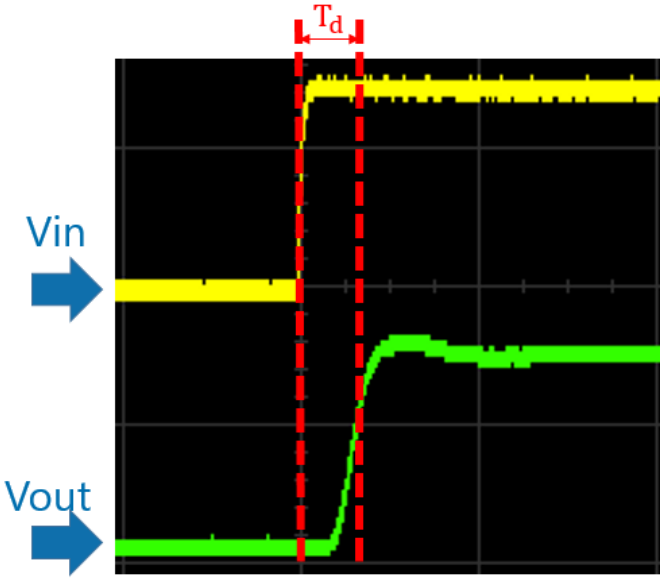

Figure 2-7 Step response to obtain amplifier transfer function characteristics

2.3 Noise reduction/filtering

Filters implemented in hardware/software are required in PHIL simulations to reduce the impact of noise on the PHIL simulation. The voltage and current measurement sensors, physical wiring and electromagnetic coupling between the interfaces devices introduces noise in the PHIL simulation which impacts the accuracy and stability of the simulation. The errors introduced by noise can be increasingly amplified in the interface until the hardware limits on the interface devices are exceeded. Filters however introduce magnitude attenuation and additional delays to the PHIL simulation. The amount of time delay and signal attenuation introduced by the filter is determined by the selected filter design and filter cut-off frequency. The filter parameters should be selected to offer an acceptable trade-off between improved stability and accuracy of the PHIL simulation.

2.4 Interface algorithms (IA)

The interface algorithm determines how signals are exchanged between the RTS and the DUT. The IA can either be voltage and/or current feedback type depending on the selected amplifier. Interface algorithms for PHIL simulations include [1]:

2.4.1 Ideal Transformer Method (ITM)

The ITM method is the most commonly used IA due to its high accuracy, low computation requirements and ease of implementation. The ITM works on voltage/current amplification and current/voltage feedback.

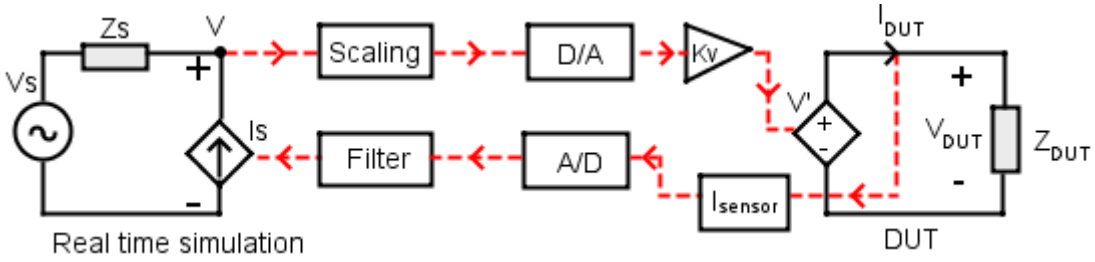

Figure 2-8 Voltage Type: Ideal Transformer Method

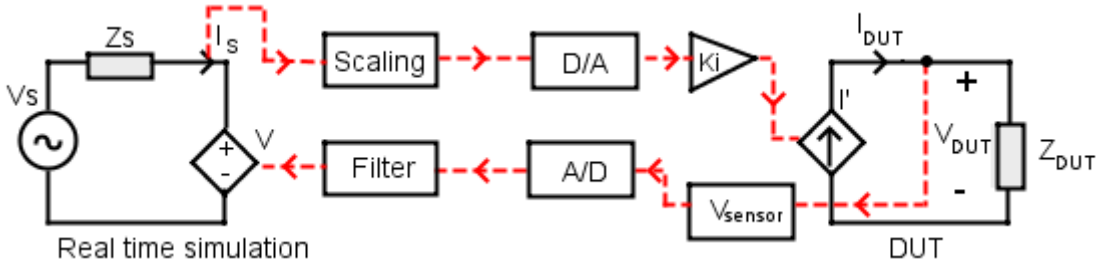

Figure 2-9 Current Type: Ideal Transformer Method

The open loop transfer function of the ITM is given by:

$$Go_{ITM\_voltage} = e^{-s\Delta T_d}\frac{Z_s}{Z_{DUT}}\,T_{amp}(s)T_{filt}(s) \tag{2.1}$$

$$Go_{ITM\_current} = e^{-s\Delta T_d}\frac{Z_{DUT}}{Z_S}T_{amp}(s)T_{filt}(s) \tag{2.2}$$

Where:

- ΔT_d is the total time delay in the PHIL interface.
- Z_s is the equivalent impedance of the network in the RTS.
- Z_{DUT} is the impedance of the device under test.
- T_{amp} is the transfer function of the amplifier
- T_{filt} is the transfer function of the filter
- K_v/K_i is the gain of the voltage/current amplifier

From the open loop transfer function, the stability of the voltage and current type ITM is largely determined by the magnitude of the impedance ratio and the total time delay as shown by the Nyquist criteria in Figure 2.10. To avoid instability using the ITM interface, the impedance ratio should satisfy the following criteria:

$$\text{Voltage ITM: } \left|\frac{Z_s}{Z_{DUT}}\right| \leq 1 \tag{2.3}$$

$$\text{Current ITM: } \left|\frac{Z_{DUT}}{Z_s}\right| \leq 1 \tag{2.4}$$

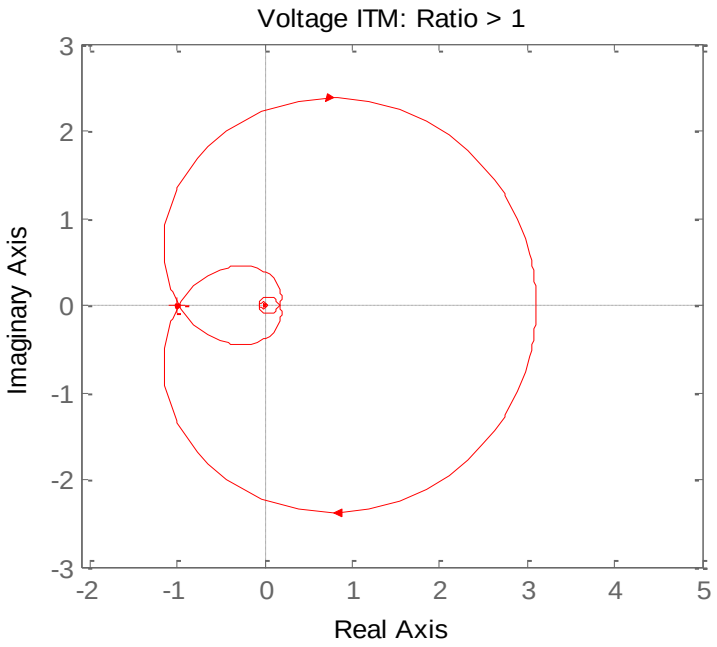

Figure 2-10 Nyquist Criteria of Voltage ITM

2.4.2 Transmission Line Method (TLM)

The TLM uses a linking inductor or capacitor to interface the RTS with the DUT.

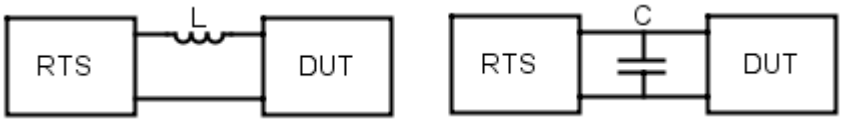

Figure 2-11 Linking component separating RTS and DUT

The inductor or capacitor is taken as a Bergeron transmission line and modeled as an equivalent Norton circuit or Thevenin circuit. The equations of the TLM method are given by:

$$Z_{lk} = \frac{L}{\Delta T_d} \; or \; Z_{lk} = \frac{\Delta T_d}{C} \tag{2.5}$$

$$V_1 = V_{DUT}(t - \Delta T_d) + Z_{lk} I_{DUT}(t - \Delta T_d) \tag{2.6}$$

$$V_2 = V(t - \Delta T_d) + Z_{lk} I_s(t - \Delta T_d) \tag{2.7}$$

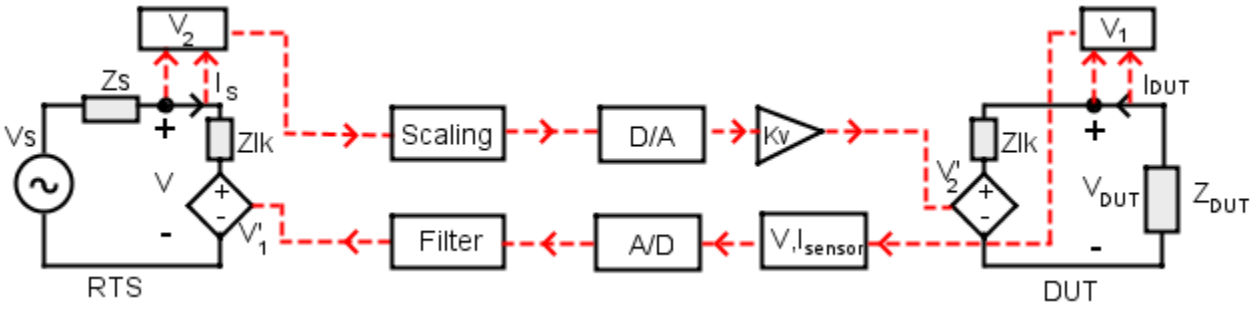

Figure 2-12 Transmission Line Method – Thevenin Equivalent

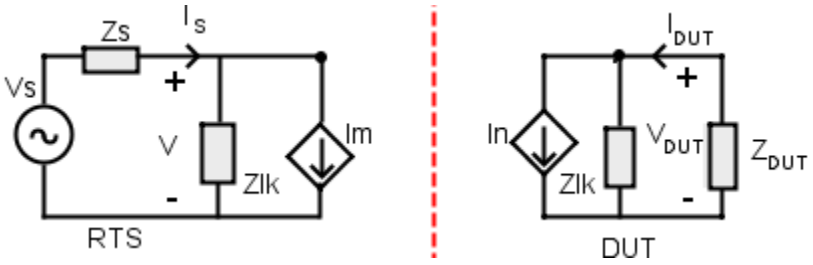

Figure 2-13 Transmission line method - Norton Equivalent

Where:

ΔT_d is the travel time of the transmission line which becomes the total time delay in the PHIL simulation.

The open loop transfer function of the TLM is given by:

$Go_{TLM} = \frac{1-\beta e^{-2s\Delta T_d}}{1+\beta e^{-2s\Delta T_d}} \frac{Z_s}{Z_{lk}} T_{amp}(s) T_{filt}(s)$	(2.8)
$\beta = \frac{Z_s - Z_{lk}}{Z_s + Z_{lk}}$	(2.9)

For stability of the TLM, the time delays introduced by the D/A, A/D, amplifier, sensors and filters should be taken into consideration when selecting the minimum length of the interface transmission line.

$$\tau = \Delta T_d = length(km) * \sqrt{L\left(\frac{H}{km}\right) * C\left(\frac{F}{km}\right)} \quad (2.10)$$

$$length\ (km) = \tau\ (\mathrm{s}) * speed\ of\ light\ \left(\frac{km}{s}\right) \quad (2.11)$$

$$\tau\ >\ T_{D/A} + T_{A/D} + T_{amp} + T_{filt} + T_{sensors} + \Delta T_{time\_step} \quad (2.12)$$

The TLM is highly stable due to the use of trapezoidal integration but its limitations include [1]:

- Reduced accuracy due to power loss in the linking impedance. The power loss in Z_{lk} must be taken into account when sizing the power amplifier.

- Assuming a fixed total time delay introduces errors in the PHIL results as the total time delay varies with the test conditions and the frequency of the PHIL simulation.
- The wiring of the linking impedance introduces more complexity in the PHIL implementation. The linking impedance must be properly sized and changed whenever the circuit configuration changes reducing the flexibility of the TLM.

2.4.3 Partial Circuit Duplication (PCD)

The partial circuit duplication method includes a linking impedance Zab in the simulated system and also on the hardware side. Large values of the linking impedance improves the stability of the interface but introduces inaccuracies due to increased power losses. The open loop transfer function of the PCD method is given by [1]:

$$Go_{PCD} = \frac{Z_s Z_{DUT}}{(Z_s+Z_{ab})(Z_{DUT}+Z_{ab})} e^{-s\Delta T_d}\, T_{amp}(s) T_{filt}(s) \tag{2.13}$$

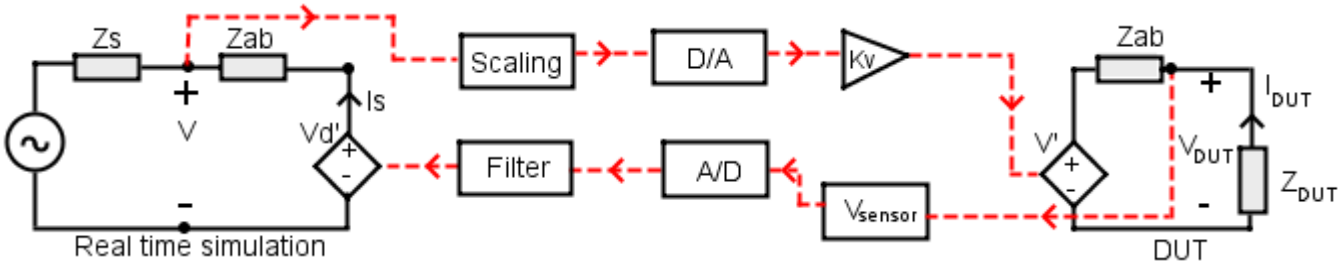

Figure 2-14 Partial Circuit Duplication

2.4.4 Damping Impedance Method (DIM)

The damping impedance method has a linking impedance Z_{ab} similar to the PCD and includes a damping impedance Z_{damp}. The DIM has very high stability when the value of Z_{damp} is equal to Z_{DUT}. The open loop transfer function of the DIM method is given by [1]:

$$Go_{DIM} = e^{-s\Delta T_d} \frac{Z_s(Z_{DUT} - Z_{damp})}{(Z_s + Z_{damp} + Z_{ab})(Z_{DUT} + Z_{ab})}\, T_{amp}(s) T_{filt}(s) \tag{2.14}$$

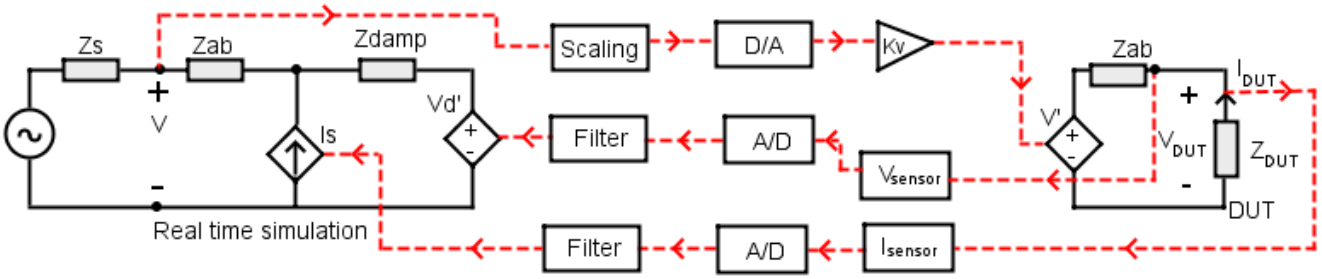

Figure 2-15 Damping Impedance Method

3 Characterizing the PHIL interface

Since the loading of the amplifier affects the stability of the PHIL interface, it is recommended to characterize the interface to obtain the required gains, amplifier behaviour, noise errors of the measurement sensors and the time delays. The amplifier discussed in this section is the PAS 1000 amplifier by Spitzenberger and Spies.

3.1 Amplifier gain

The PAS 1000, 4-quadrant power amplifier can be operated in AC or DC mode in the following voltage ranges 60V, 150V, 300V and 630V (DC only). To confirm the gains of each voltage range in AC mode, a sine wave was sent out using the analogue output card (GTAO). A scale factor given by (1) was applied to the simulated sine wave to ensure the output sine wave is within the input voltage of +/-5 volts peak.

From (1), for $|\mathbf{V}\text{simulated}| = |\mathbf{V}\text{gtao\_out}|$, the scale factor is given as 5. The procedure was repeated for the DC mode with a step signal simulated in the RTDS.

$$\mathbf{Scale\ Factor}_{\mathbf{GTAO}} = \frac{|\mathbf{V}\text{simulated}| * \mathbf{5}}{|\mathbf{V}\text{gtao\_out}|} \tag{2.15}$$

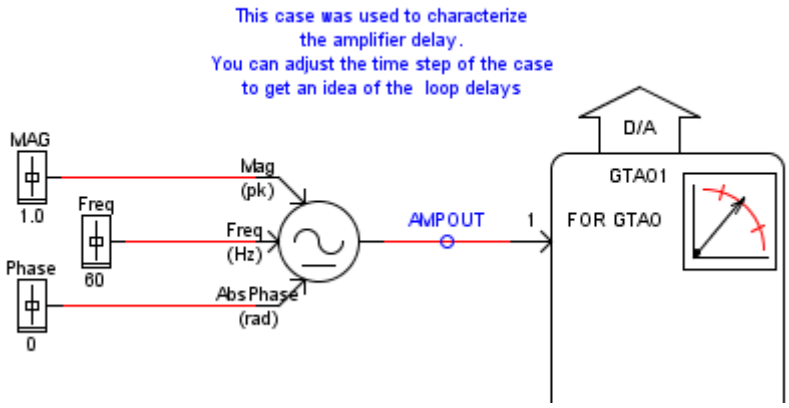

Figure 3-1. RSCAD case for amplifier gain testing

The analog output signal from the GTAO was then applied as input to the amplifier as shown in figure 2.

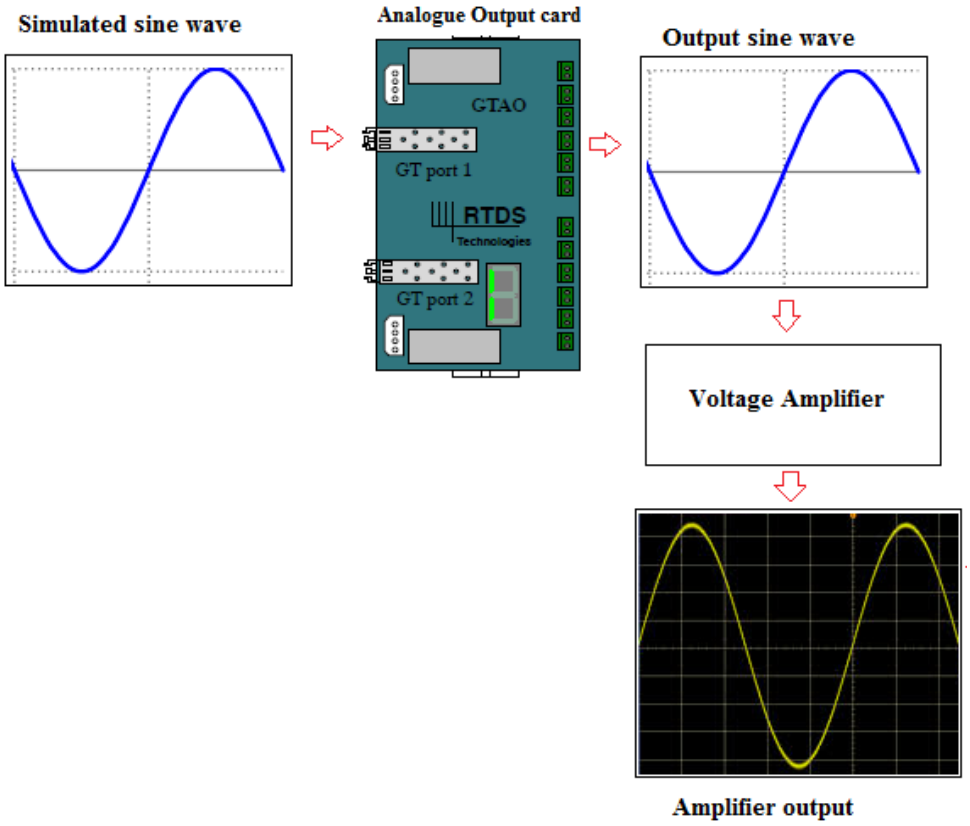

Figure 3-2 Amplifier gain testing

The amplifier gain measured by (2.16) are shown in Table 3-1:

$$\boldsymbol{Gain} = \frac{|\mathbf{V}\text{amp\_out}|}{|\mathbf{V}\text{gtao\_out}|} \tag{2.16}$$

Table 3-1 Amplifier gain - AC and DC mode

Voltage range (AC and DC)	**(~) gain (V/V)**
60V	17
150V	43
300V	85
630V (DC only)	126

3.2 Interface noise, time delay and stability characteristics

The accuracy and stability of the PHIL simulation depends on the selected interface algorithm as well as knowledge of the time delay and noise between the interfaced devices. From Figure 3-2, the output sine wave from the GTAO card was applied to the external input channels of the amplifier and the amplifier output voltage channel monitored on an oscilloscope. Figure 3-3 shows the amplifier output voltage signal has noise superimposed on the signal. To further analyze the noise, the external input signals were shorted and the voltage monitor channel observed on an oscilloscope as shown in Figure 3-4, the high frequency noise on the measurement sensors introduced to the PHIL interface has a voltage level of 500mV.

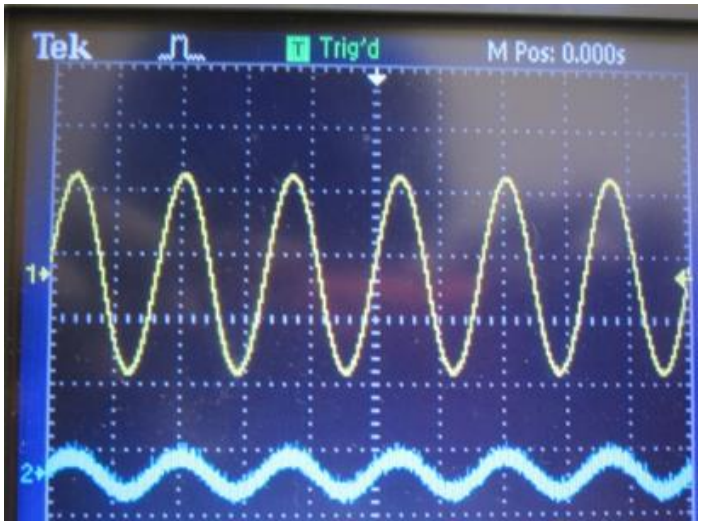

Figure 3-3 Blue curve is the monitored amplifier monitor voltage channel, yellow curve is the GTAO output sine wave applied to the amplifier's external input channels. Note the measurement ratio is 1V:100V

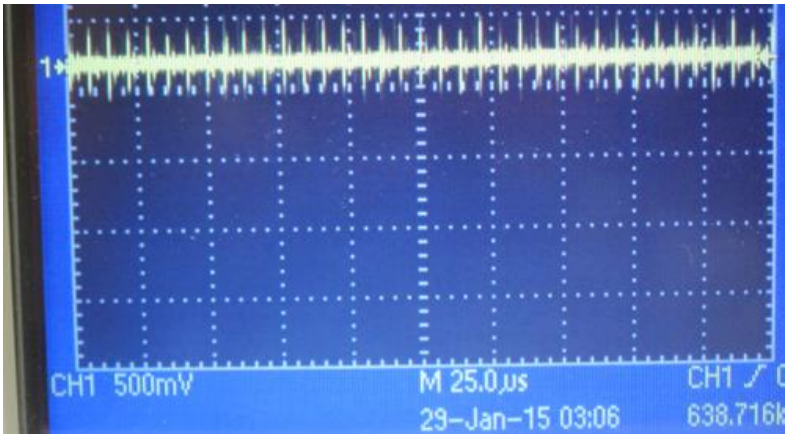

Figure 3-4 Interface noise on voltage output channels

As a further test, the output of the amplifier which will be applied to the hardware under test was monitored to check for a similar noise situation but it was observed that the output signal at the back of the amplifier did not

have the same high frequency noise compared to the signal from the amplifier's monitor channels as shown in figure 3-5.

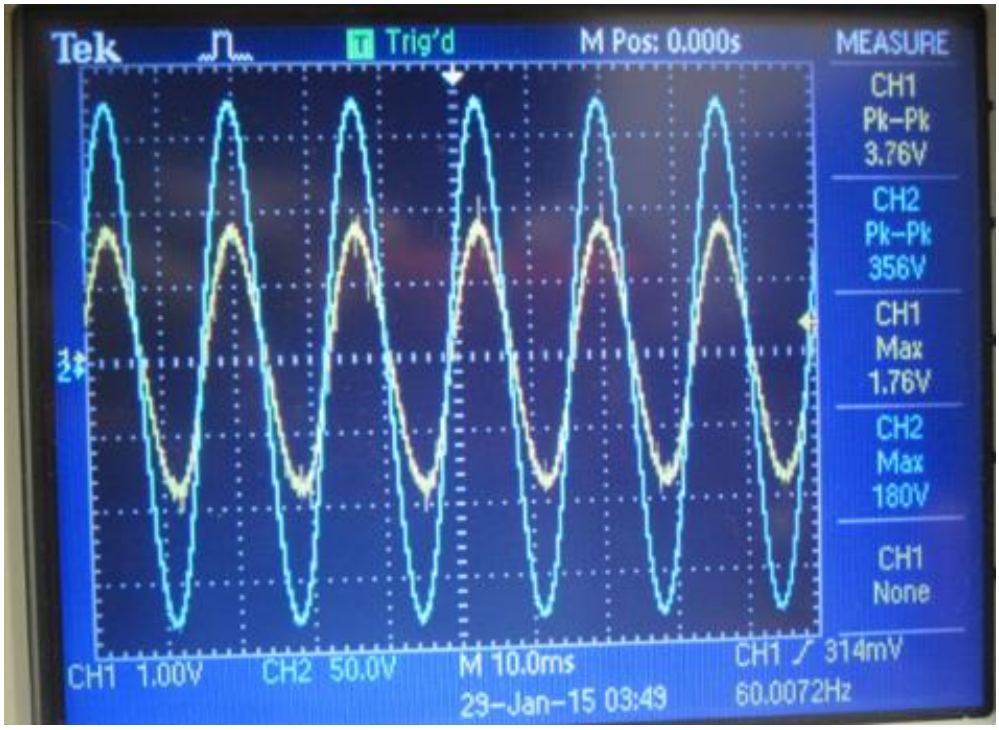

Figure 3-5 Blue curve is amplified voltage signal, yellow curve is the voltage on the monitor channels.

As the measured signals of voltage and current from the amplifier's monitor channels will be sent back to the simulation, filtering techniques are required to reduce the high frequency interface noise to ensure accuracy and stability of the PHIL simulation. Hardware and/or software filters could be implemented to further reduce the noise introduced by the PHIL interface.In addition, using shielded cables to connect the amplifier's voltage and current monitor channels to the RTDS will help reduce electromagnetic noise coupling from surrounding electrical equipment. The monitor voltage signal from the amplifier was then sent back to the simulation using the gigabit transceiver analogue input card (GTAI). The GTAI card has 12 differential input channels, for clarity only two input channels are shown in figure 3-6, and require a +signal, -signal and ground reference connection. Differential inputs are used to minimize common mode noise and eliminate DC offsets between the external equipment and the RTDS. A 1k-ohm resistor is used to connect the single ended output of the amplifier to the GTAI channel. The input voltage range of the GTAI channels is +/- 10Volts.

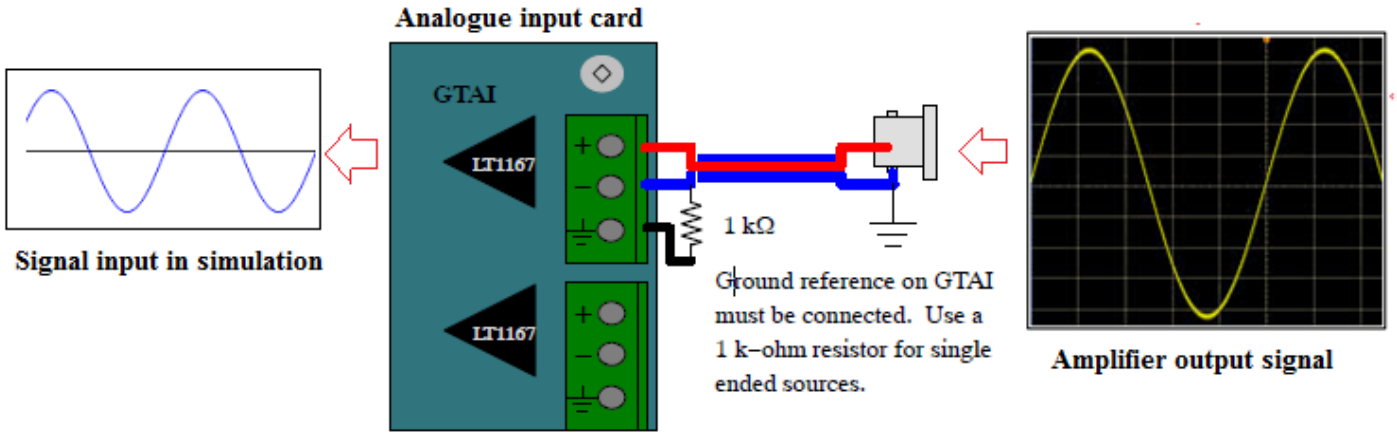

Figure 3-6 Amplifier output sent to simulation using GTAI card

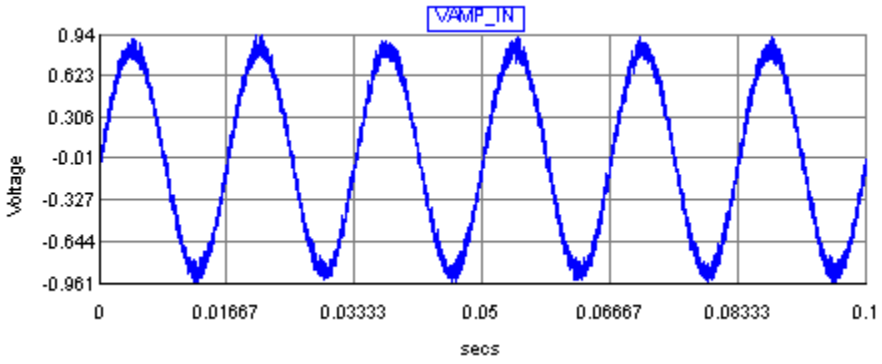

Figure 3-7 Amplifier voltage (blue curve) monitored in simulation

To filter the high frequency noise on the input signal (VAMP_IN) monitored in the simulation, the cut-off frequency of the anti-aliasing filter on the GTAI channel was reduced from 84.2 kHz to 10.1 kHz by moving the jumpers as shown in figure 3-8.

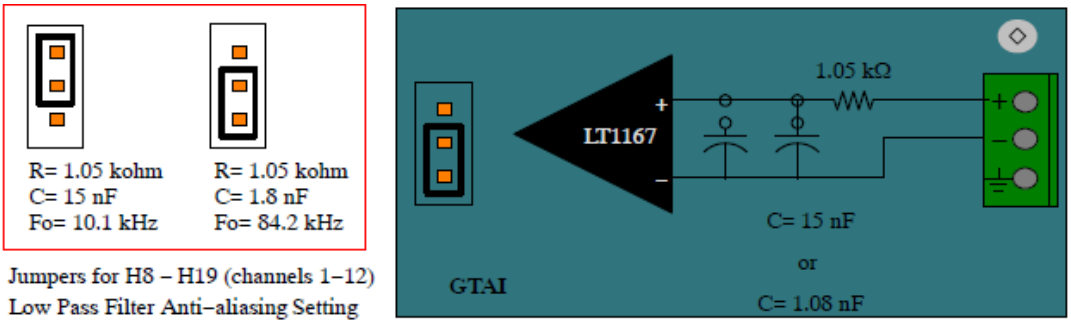

Figure 3-8 Anti-aliasing filter on GTAI channels

Figure 3-9 shows the monitored signal in the RTDS simulation has a reduced noise component with the filter cut-off set to 10.1kZ. This however introduces more phase shift on the sampled signal. Table 3-4 shows the introduced phase shift of the 10.1 kHz and 84.2 kHz filters for a sine wave of 60Hz and a time step of 50usecs.

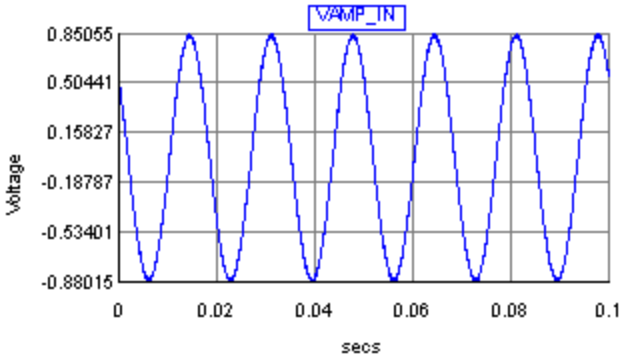

Figure 3-9 Noise reduced on monitored signal in simulation

Table 3-2 Phase shift and delay of anti-aliasing filter

Cut-off frequency(kHz)	Phase Shift (deg)	Delay (usecs)
10.1	0.3402	15.75
84.2	0.0408	1.890

NOTE: For main power system simulation with a time step of 50usecs, the 10.1 kHz cut-off frequency offers a compromise between noise reduction and introduced delay. However if the GTAI is providing signal into the small time step simulation (1 – 3usecs) then the 84.2kHz cut-off frequency should be selected.

3.2.1 Time delay and Stability of closed loop simulation using a resistive load.

A simple voltage circuit is used to characterize the time delay and stability of the HIL interface. The circuit of figure 3-11 the PHIL interface of the voltage divider circuit using the ITM method. The load R2 represents the hardware under test to be interfaced to the simulator at the node point V.

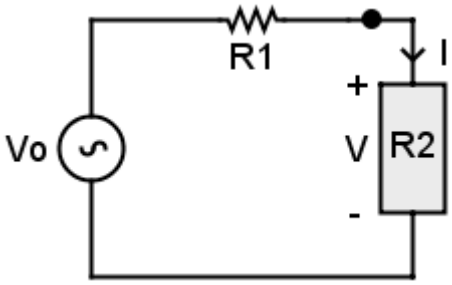

Figure 3-10 Voltage divider circuit

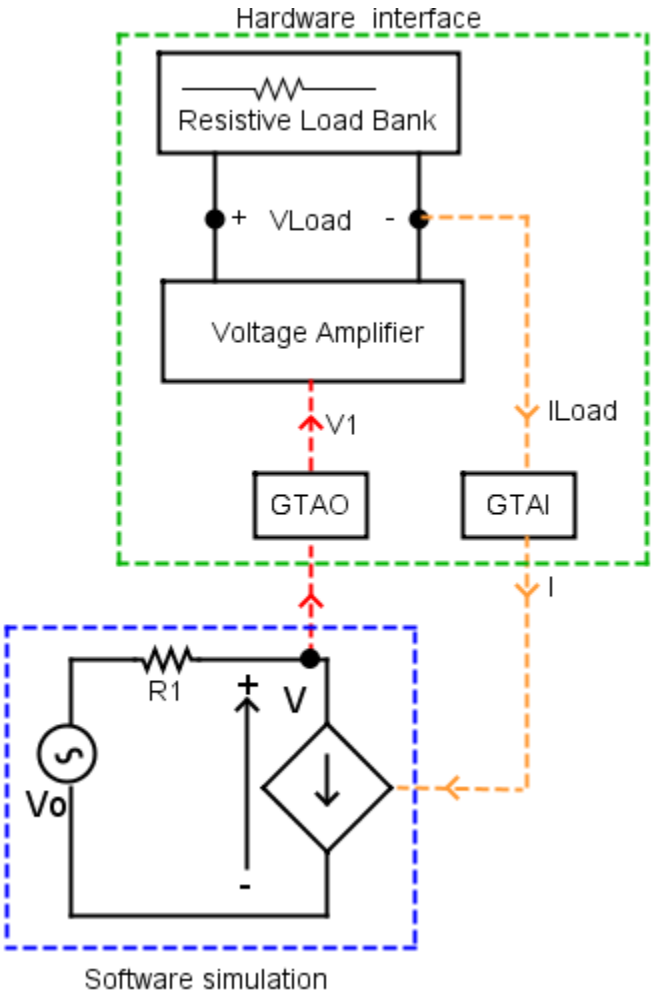

Figure 3-11 Hardware-Software PHIL Ideal Transformer Interface

A 5kW, 110Vdc resistive load bank was connected to the amplifier's output. The load bank has switchable resistance values at power ratings of 0.5kW, 1kW, 1.5kW and 2kW. The time delay between the voltage "V" and current "I" signals is measured in the simulation as the difference between the zero crossings when a negative to positive transition occurs.

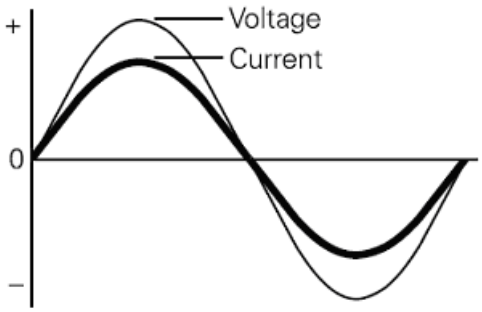

Figure 3-12 Measure signal delay between voltage V and current I

3.2.1.1 Simulation results

Case A: R1= R2= 25.8 ohms. Vsource = 5kV rms, anti-aliasing filter = 84.2kHz, time step = 50usecs

This is an unstable situation as the ratio of the simulated and hardware impedance is greater than 1. When the loop was closed, the following error was observed in the amplifier **"I2C-BUS-ERROR 1040 --- press ENTER". The amplifier tripped the output and the measured bus voltage on the amplifier showed 85.0V.** The simulation results are shown in figures 3-15 – 3-16.

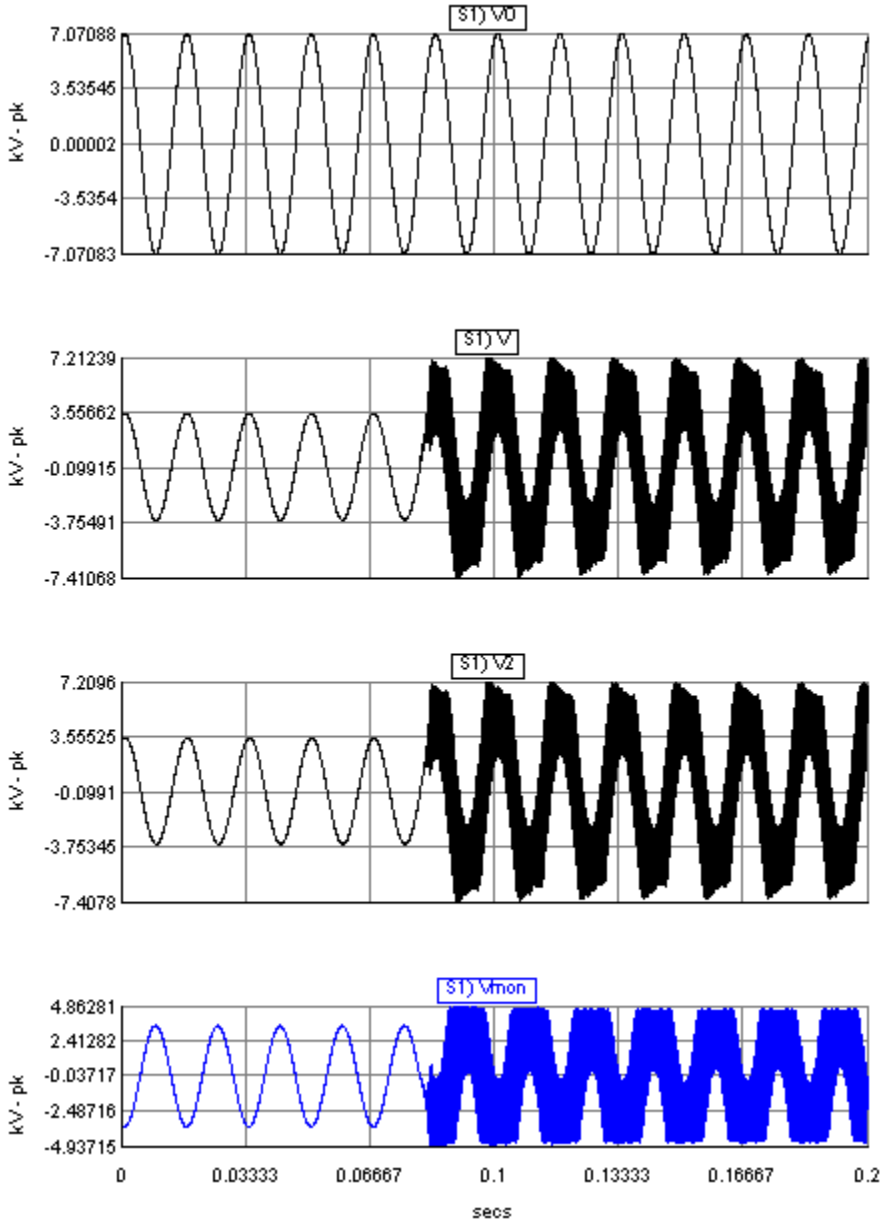

Figure 3-13 Case A Voltages

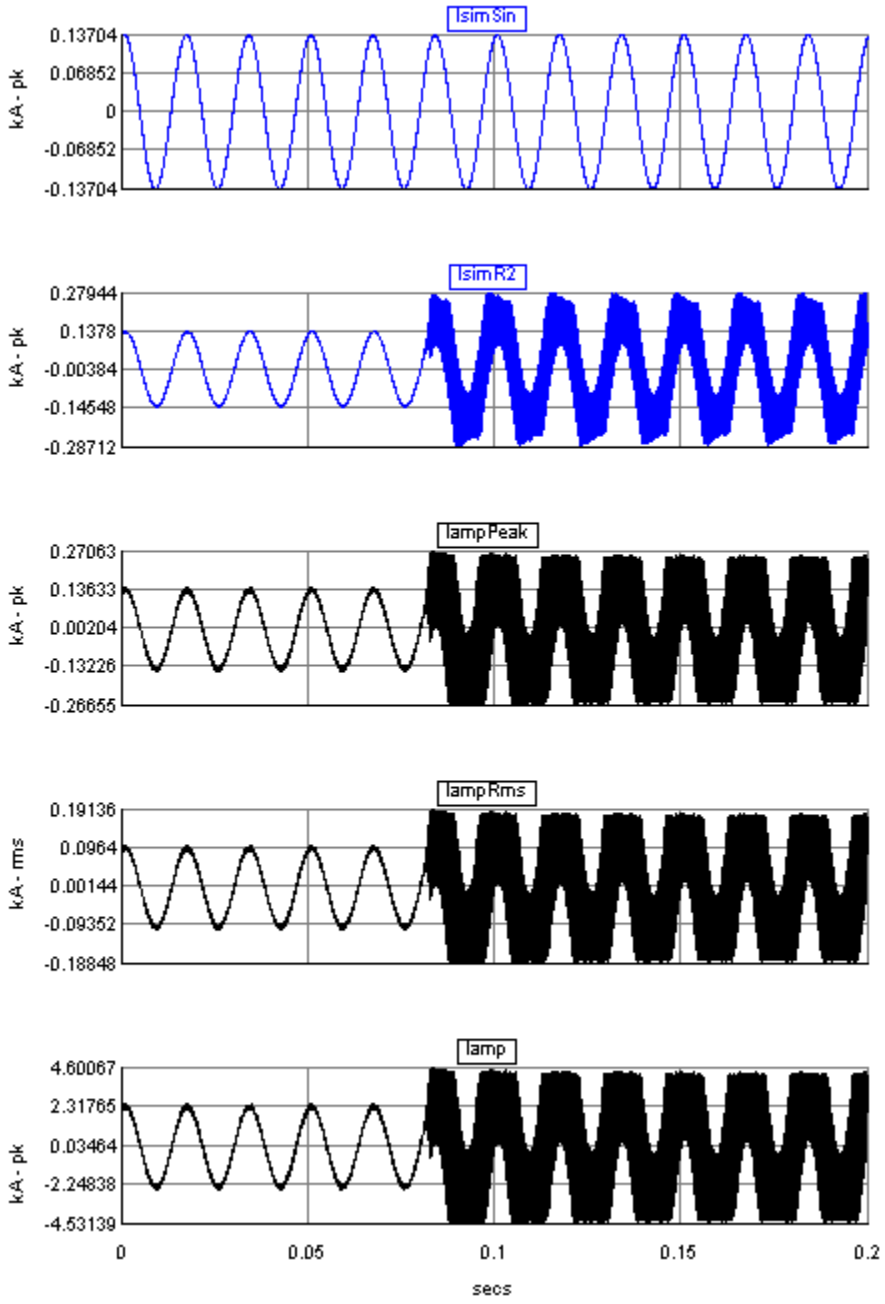

Figure 3-14 Case A Currents

Case B: R1= 5 ohms R2= 25.8 ohms. Vsource = 0.5kV rms, anti-aliasing filter 10.1 kHz, time step = 50usecs

This is a stable situation as the ratio of the simulated and hardware impedance is less than 1. With the anti-aliasing filter set to 10.1kHz there is reduced noise on the feedback current from the measurement sensors.

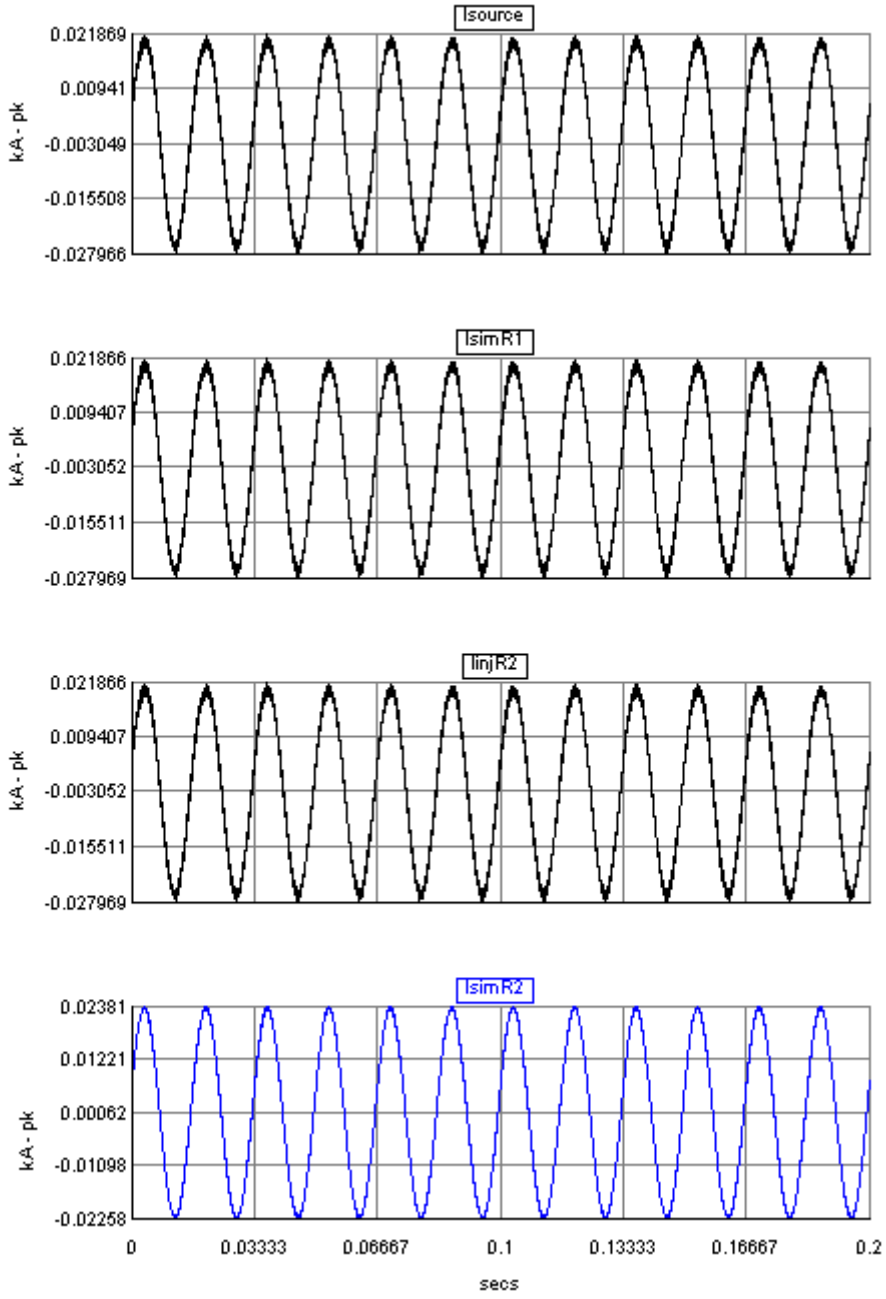

Figure 3-15 Case B Currents

3.2.2 Stability and Accuracy of the PHIL Interface

A suitable method to evaluate the stability and accuracy analysis of the PHIL application is to simulate the interface in a software environment before implementing the physical power hardware in the loop setup. The block diagram of the PHIL interface of the voltage divider circuit using the ITM is shown in Figure 3-17.

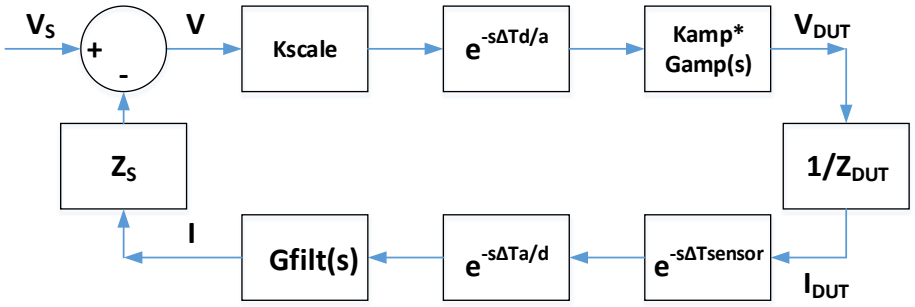

Figure 3-16 Block diagram of ITM

A first order approximation is used to model the linear amplifier given by:

$$G_{amp} = \frac{1}{1+sT_{amp}} \tag{3.2}$$

Where: (3.3)

$$T_{amp} = R_{amp}C_{amp} = \frac{1}{2\pi f_{bandwidth(3dB)}}$$

Where the open loop transfer function using a first order filter becomes: (3.4)

$$G_{loop} = \frac{\omega_o^2 e^{-sT_d}}{s^2+2\zeta\omega_o s+\omega_o^2} * \frac{Z_s}{Z_{DUT}} = e^{-sT_d} \frac{1}{(T_f T_{amp})s^2+(T_{f+}T_{amp})s+1} * \frac{Z_s}{Z_{DUT}}$$

The software simulation of the ITM interface using the voltage divider is shown in Figure 3-18 with the time delay set to 2 times the simulation time step.

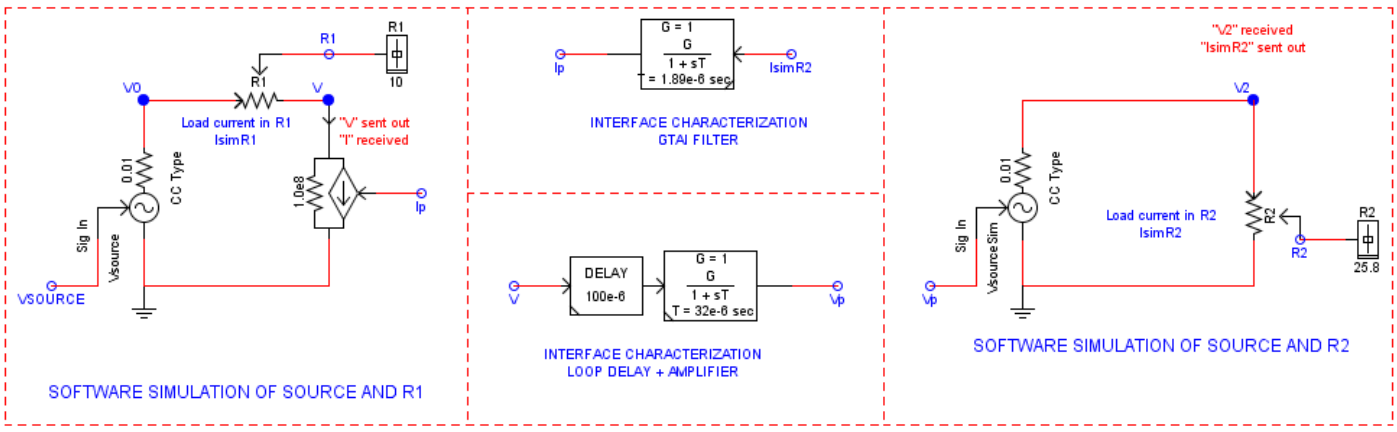

Figure 3-17 Software simulation of PHIL interface

For the same resistance values as Case A, the software simulation of the interface shows the same instability at the point the loop is closed. Software simulations help to define the limits of the PHIL interface and evaluate the accuracy. The challenge, as mentioned in the previous section, is that detailed information of the device under test is usually not available from manufacturers making it difficult to obtain a sufficient stability and accuracy evaluation of the PHIL interface.

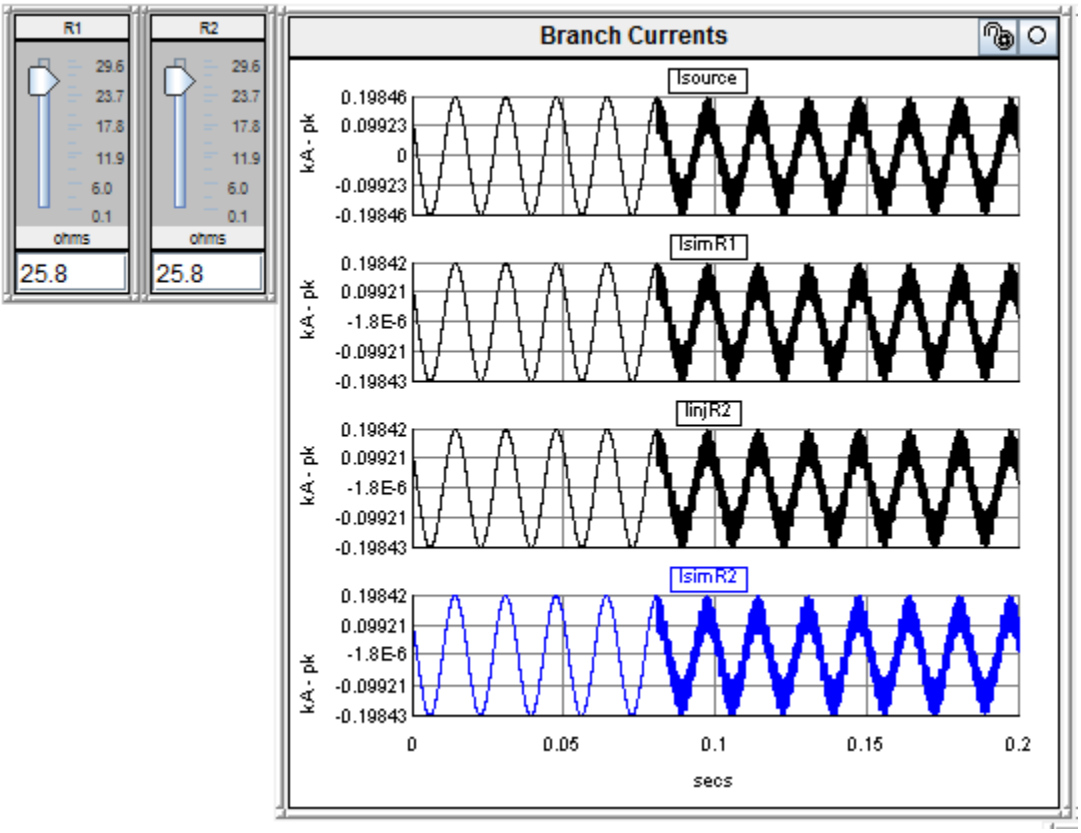

Figure 3-18 Software simulation of PHIL interface showing instability

3.2.3 PHIL Interface using the small time step bridge box

The stability of the voltage ITM can be increased by reducing the loop delay. As shown in Figure 3-19 the Nyquist criteria shows the unstable region is not circled with the impedance ratio greater than 1 when the time delay is reduced from 100µsecs to 4µsecs compared to Figure 2-10. The time delay can be reduced using the small time step bridge box in RSCAD which keeps the time step between 1.5µsecs-3µsecs. Stricter node limitations and limited model availability restrict the size of the simulated network in the small time step. For more information, the reader is referred to the small time step simulation manual of the RTDS.

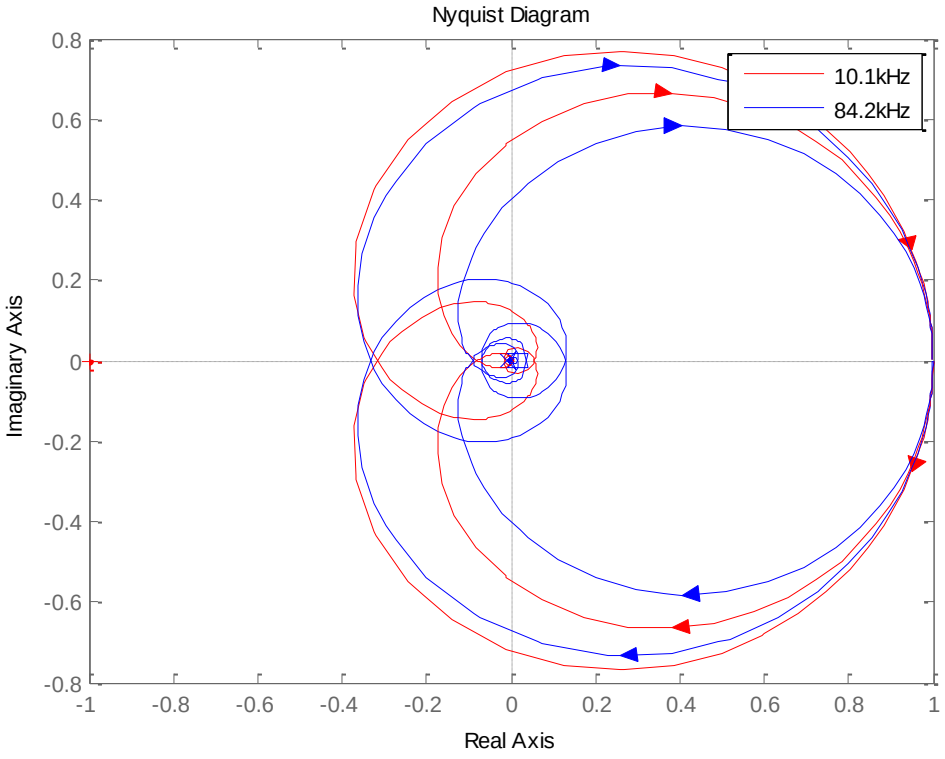

Figure 3-19 Nyquist criteria of ITM showing improved stability with 2useconds delay

The voltage divider circuit of Figure 3-11 was simulated in the small time step environment with a time step of 1.93µsecs as shown in Figure 3-20. In the small time step, stable closed loop operation was obtained when $\frac{R1=25.8}{R2=25.8}$ as shown in Figure 3-21.

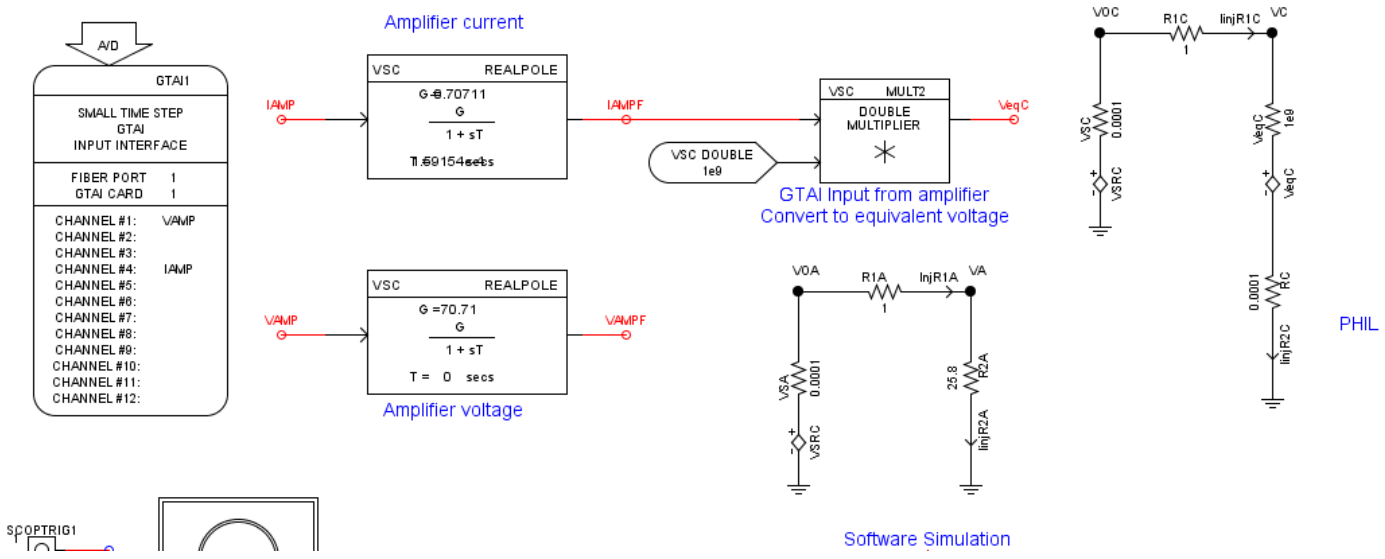

Figure 3-20 PHIL interface of voltage divider in smalll time step

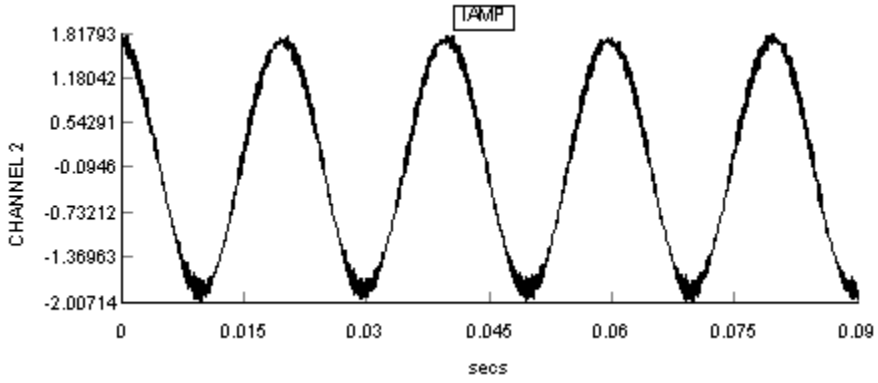

Figure 3-21 Unfiltered closed loop current signal from small DT GTAI channel

4 PHIL Interface with a PV Micro inverter

A test setup of a PHIL interface with a 255W PV inverter and the SPS amplifier is shown in Figure 4-1. The DC side of the inverter is connected to a solar panel with a metal halide light source used as a sunlight simulator. The AC side of the inverter is connected to the amplifier output terminal which provides the grid simulation at 240Vrms, 60Hz. The inverter current measured by the amplifier is sent back to the simulated grid in the RTS.

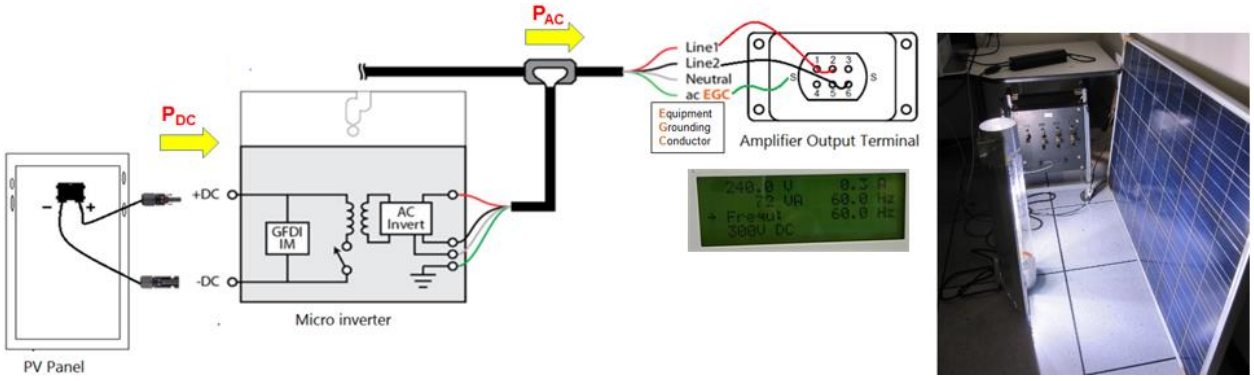

Figure 4-1 PHIL interface with PV Inverter

Figure 4-2 shows that the inverter current observed in the RTS is super imposed with noise from the PHIL interface. A low pass filter is used to eliminate the noise on current signal. The filter improves the stability of the PHIL simulation but attenuates the magnitude of the current signal and adds an additional time delay. The magnitude attenuation and time delay introduced by the filter is determined by the selected cut off frequency. Lower cut-off frequencies result in higher time delays and increased magnitude attenuation which impacts the accuracy of the PHIL simulation observed in the RTS.

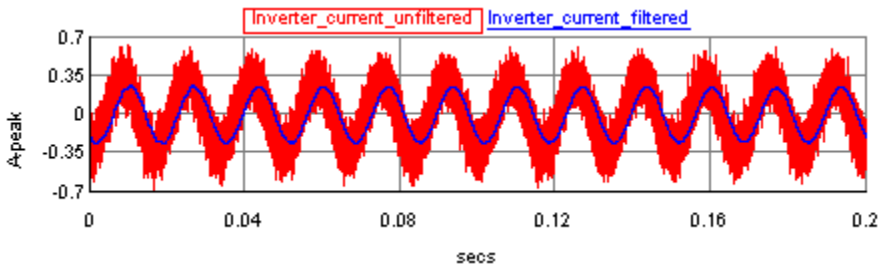

Figure 4-2 Inverter current in the RTDS

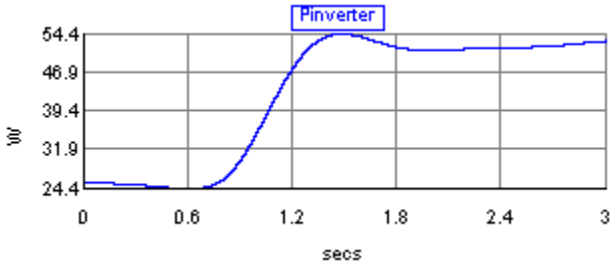

Figure 4-3 Inverter power observed in the RTS increases by 50% when filter cutoff is changed from 500Hz to 5kHz.

Figure 4-3 shows the inverter response to a line to ground fault simulated in the RTS. The current response shows that the inverter remains grid-connected when the fault duration is 5 cycles. The point at which the inverter disconnects from the grid can be seen when the fault duration was increased to 60 cycles. It should be noted that the contingency scenarios to be tested in the PHIL interface should be within the protection limits of the device under test as well as the amplifier ratings to prevent unstable operation.

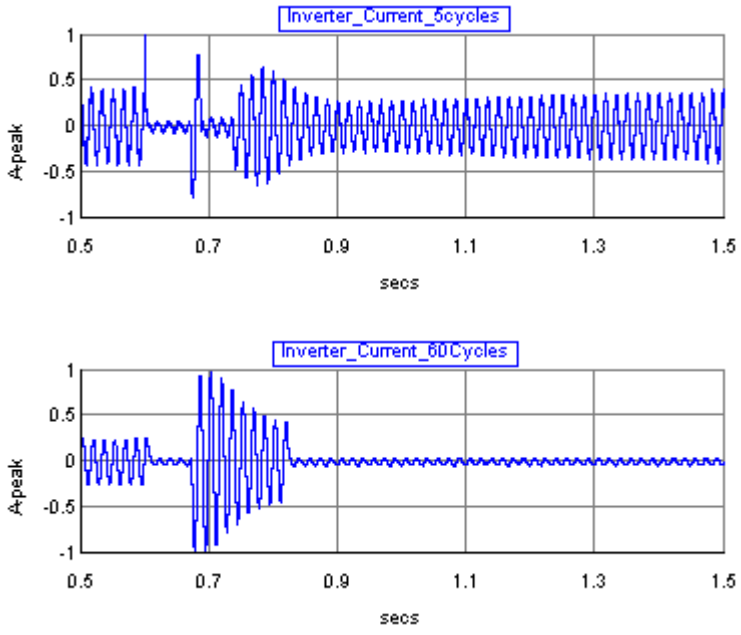

Figure 4-4 Inverter AC current response to a 5 cycle and 60 cycle, line to ground fault condition simulated in the RTS

5 Reference

Comparison of PHIL Interface Algorithms

[1] Wei Ren; Steurer, M.; Baldwin, T.L., "Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms," *Industry Applications, IEEE Transactions on* , vol.44, no.4, pp.1286,1294, July-aug. 2008 doi: 10.1109/TIA.2008.926240

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Comparison of multiple Power Amplification Types for Power Hardware in the Loop Applications

[3] Lehfuss, F.; Lauss, G.; Kotsampopoulos, P.; Hatziargyriou, N.; Crolla, P.; Roscoe, A., "Comparison of multiple power amplification types for power Hardware-in-the-Loop applications," *Complexity in Engineering (COMPENG), 2012* , vol., no., pp.1,6, 11-13 June 2012 doi: 10.1109/CompEng.2012.6242959